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Printed Electronics

Ink-Jet Printed CMOS Electronics from Oxide Semiconductors

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Complementary metal oxide semiconductor (CMOS) technology with high transconductance and signal gain is mandatory for practicable digital/analog logic electronics. However, high performance all-oxide CMOS logics are scarcely reported in the literature; specifically, not at all for solution-processed/printed transistors. As a major step toward solution-processed all-oxide electronics, here it is shown that using a highly efficient electrolyte-gating approach one can obtain printed and low-voltage operated oxide CMOS logics with high signal gain (≈21 at a supply voltage of only 1.5 V) and low static power dissipation.

1. Introduction

High noise immunity and low static power consumption of complementary metal oxide semiconductor (CMOS) technology, comprising symmetrical pair of *n*-type (NMOS) and *p*-type metal oxide semiconductor (PMOS) field-effect transistors (FETs), are the key factors behind the development of logic electronics. Over the last 50 years CMOS technology has led to increasing speed and packing density of FETs in microprocessors, which in turn facilitated the realization of various modern-day portable electronic devices.[1–5] On the other hand, solution-processed or printed logics have recently been in high demand in application areas that are beyond silicon electronics. In this context organic semiconductors have always been the first choice due to their easy solution processability.[6] Although there was an initial scarcity of suitable *n*-type organic semiconductors, presently the performance of the *p*-type and *n*-type FETs can nearly be matched; as a result, there are copious examples of solution-processed organic CMOS circuits.[7–10] Nevertheless, organic devices still have problems with environmental stability; moreover, their field-effect mobility values are rather low and may not be sufficient for all the anticipated applications.[11] Consequently, efforts to realize solution-processed oxide electronics have been initiated in the last few years. Here, the important point is that the oxide semiconductors are largely gifted with much superior electronic transport properties (which are usually reflected in their high intrinsic carrier mobility, sometimes order of magnitude higher than their organic counterparts), high environmental stability, and high transparency. All these strong advantages have shifted a considerable part of the research efforts in printed electronics toward oxide FETs.[12–15] However, there are also obstacles to overcome for oxide electronics, one of them is the virtual absence of high performance *p*-type semiconductors; as a result, there has been hardly any report published on solution-processed all-oxide CMOS logics till date. In this regard, here we present a systematic study on printed, all-oxide CMOS electronics, where

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the NMOS and PMOS FETs are composed of precursor derived indium oxide (In_2O_3) and copper oxide (CuO) thin films, respectively. The performance of the PMOS transistors is found to be reasonably good; however, of course, inferior compared to the reported NMOS devices. Nevertheless, we demonstrate that our printed CMOS inverters and common-source amplifiers can operate at extremely low supply voltages and show reasonably high signal gain and nominal static power dissipation.

2. Results and Discussion

Indium oxide is an electron conducting, high intrinsic mobility (≈160 $cm^2 V^{-1} s^{-1}$),[16] high band gap (3.5 eV) transparent semiconductor with high environmental stability. It is also very easy to prepare as a phase-pure material, following solution-based synthesis routes. In contrast, copper oxide is reportedly a reasonably good *p*-type oxide semiconductor, however, with an intrinsic charge carrier mobility value of only 0.01 $cm^2 V^{-1} s^{-1}$.[17]

Structural characterization is performed on the printed films, which have undergone the same annealing conditions as the real devices. The grazing incidence X-ray diffraction (GIXRD) has been used as a tool to monitor decomposition of the precursor salts and formation of desired oxide phase as a function of annealing temperatures. **Figure 1**a,b shows XRD studies performed on the In_2O_3 and CuO precursors that have undergone different heat treatments. The XRD pattern of the CuO precursor film heated at 150 °C already shows decomposition of the precursor to metallic Cu, whereas the In_2O_3 precursor does not show any detectable decomposition product even at 200 °C and directly transforms to single phase In_2O_3 at 300 °C (in fact a first hint of the In_2O_3 phase shows up at 230 °C, see Figure S2, Supporting Information). It has earlier been reported that pure copper can be synthesized by polyol method (where polyols such as ethylene glycol, glycerol, etc., can act as reducing agents) at very low temperatures.[18] However, In_2O_3 precursor does not decompose to metallic indium in this process at low temperatures, and In_2O_3 nanocrystals directly nucleate above 200 °C. In fact, this different decomposition behavior of In_2O_3 and CuO precursors resulted in a large variation in the film morphology between the printed and annealed In_2O_3 and CuO layers. While the crystalline In_2O_3 directly forms as the decomposition product, the CuO precursor immediately decomposes to metallic copper even during a drying step on a hotplate at 150 °C, and remains predominantly metallic Cu until 300 °C, after which it oxidizes to copper oxides. The 400 °C annealed CuO film, which is used for the transistor fabrication consists of predominantly CuO (90%) with a minor admixture of Cu_2O (10%) which is also a well-known *p*-type oxide semiconductor (see Table S2, Supporting Information).

As already mentioned, the electrolyte-gating approach has been employed. A composite solid polymer electrolyte (CSPE) is used as the gate dielectric. In earlier publications it has been shown that solid polymer electrolytes can be highly suitable gate insulator for printed oxide electronics.[19–21]

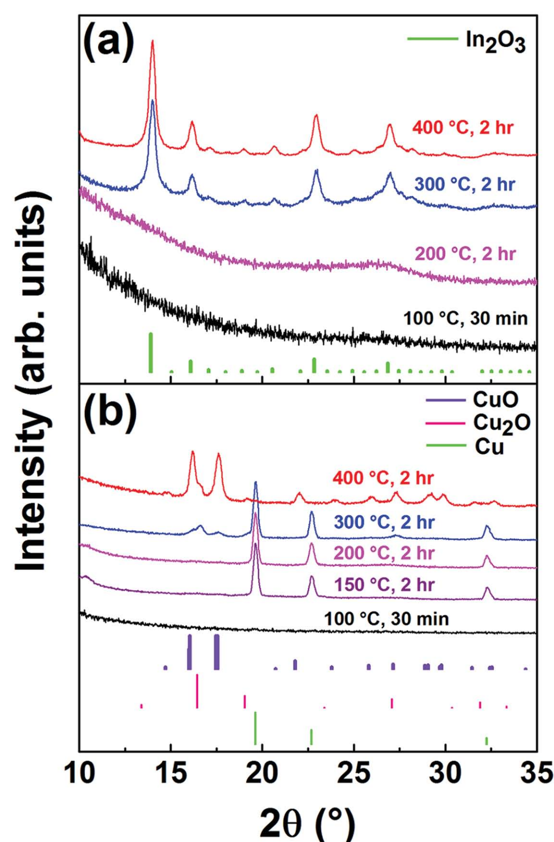

Figure 1. XRD pattern of indium oxide and copper oxide precursors, annealed at different temperatures.

Firstly, this is due to the fact that despite every optimization attempts of the semiconducting inks, their printing and post processing parameters, a printed oxide layer may possess significant surface roughness. This large surface roughness can be taken care of when an electrolyte is used as the gate insulator; in fact an electrolyte can always offer a highly conformal semiconductor/ dielectric interface.[22,23] Next, the class of polymer electrolyte used shows necessary environmental stability and sufficient thermal endurance.[24,25] Furthermore, due to the high capacitance of the electrolytic insulator, the operation voltage is reduced to ≤2 V, making such FETs and logics fully battery compatible. Finally, the rheological parameters of the chosen composite solid polymer electrolyte are ideal for the ink-jet printing; thus, the CSPE constitutes a rare example of an easily-printable high performance gate dielectric. The preparation of the CSPE is described in the Supporting Information.

The effect of the low temperature decomposition product on film morphology can clearly be observed when the microscopic images of the oxide film surfaces of In_2O_3 and CuO are compared (**Figure 2**). For the In_2O_3 precursor where indium oxide directly nucleates as the first decomposition product, the scanning electron microscopy (SEM) and atomic force microscopy (AFM) (Figure 2a,b) images show surprisingly smooth and homogeneous film morphology (which can very well be compared to a sputtered film) with a root mean square roughness (R_{rms}) value of only 0.5 nm (Figures S3 and

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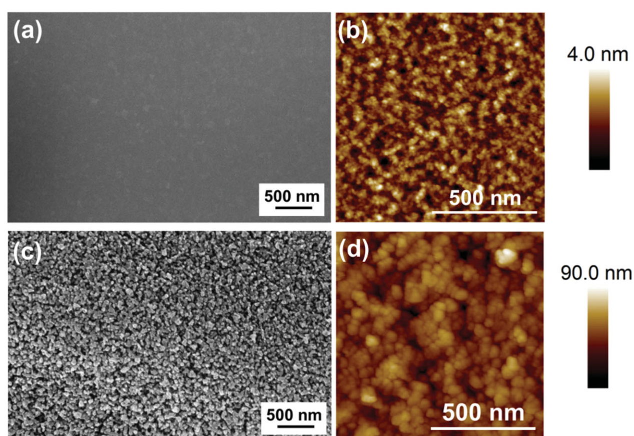

Figure 2. a,b) SEM and AFM images of indium oxide precursor and c,d) copper oxide precursors which are annealed at 400 °C for 2 h.

S4, Supporting Information). In contrast, the CuO precursor first reduces to metallic Cu and then oxidizes to CuO, with a largely different crystal volume; as a result, considerably rougher film morphology (Figure 2c,d) can be seen with R_{rms} of around 10 nm (Figures S5 and S6, Supporting Information). What is common in both printed and annealed films is the fact that a completely homogeneous, solid, and crack-free network of particles is obtained with minimal imperfections present in the films (largely due to the addition of glycerol in the precursors). Nevertheless, in case of electrolyte-gated FETs, this disparity in film morphology and surface roughness do not have a critical effect on electrical performance of the respective devices. In other words, any inferior performance of the CuO channel PMOS devices should not be correlated to the higher surface roughness. The reason is that the composite polymer electrolytes, when printed or dispensed on an oxide semiconductor with certain surface roughness/ inhomogeneity, can easily follow the rough surface with high conformity, providing an extremely smooth semiconductor–electrolyte interface at the end. In fact, the electrolytic insulator can take care of the surface corrugation even down to the nanometer level, and this feature is further corroborated here with direct evidence from the cross-section transmission electron microscopy (TEM) images. A detailed description of the preparation of the TEM cross-section samples using focused ion beam (FIB) is described in the Experimental Section. A typical TEM bright-field micrograph of indium oxide/ electrolyte interface is shown in **Figure 3**. The high resolution TEM micrograph shows crystalline indium oxide nanoparticles; the lattice spacings obtained from the associated fast Fourier transformation (FFT) pattern (red-square/ lower-right) are characteristics of In_2O_3. As can be seen in Figure 3, the indium oxide surface roughness, in the order of several nanometers, is taken care of by the printed electrolyte, which provides a completely conformal interface.

Electrical characterization of the printed transistors has been performed at ambient conditions. Transfer and current–voltage (*I*–*V*) curves of typical NMOS and PMOS devices are shown in **Figure 4**a,b and c,d, respectively. Both NMOS and PMOS transfer curves indicate accumulation mode operation with positive for NMOS (0.32 V) and negative for PMOS (–0.23 V) threshold voltages, respectively. The NMOS device shows excellent performance including high ON/OFF ratio ($\approx 10^6$), high field effect mobility (48 $cm^2\ V^{-1}\ s^{-1}$) and sharp subthreshold slope (100 mV per decade), close to the theoretical minimum (60 mV per decade).[26] In fact, as previously mentioned, indium oxide precursors (e.g., indium acetate with water and glycerol) convert to nanocrystalline In_2O_3 at annealing temperature as low as 230 °C (Figure S2, Supporting Information), and FETs that are built with this process temperature also demonstrate reasonable transistor performance with field-effect mobility of 8.3 $cm^2\ V^{-1}\ s^{-1}$ (Figure S7, Supporting Information). However, the CuO precursor unfortunately decomposes to metallic Cu first and then oxidizes to copper oxide only at 400 °C, thus limiting the possibility of preparing all-oxide CMOS electronics at lower temperatures. Moreover, the *I*–*V* characteristic curves of the PMOS devices have always shown Schottky contacts, although platinum electrodes with high work function (>5 eV) have been used. Next, in spite of the higher process temperatures, the oxide PMOS performance has always been found considerably inferior compared to the NMOS devices. It relates to the fact that the band structure of metallic oxides favors high charge carrier mobility only for electrons but not for holes. The oxygen 2p orbitals form the valence band maximum (VBM) which creates deep energy levels causing low hole mobility; whereas, the widely spread metal s orbitals form the conduction band minimum (CBM) and this leads to high electron mobility in metal oxide semiconductors.[27] Nevertheless, in our case we observed comparatively reasonable performance for the PMOS device, which includes field effect mobility of 0.22 $cm^2\ V^{-1}\ s^{-1}$, ON/OFF ratio of around 10^3, and a subthreshold slope of 600 mV per decade. The field-effect mobility values for NMOS and PMOS transistors are calculated using the following equation

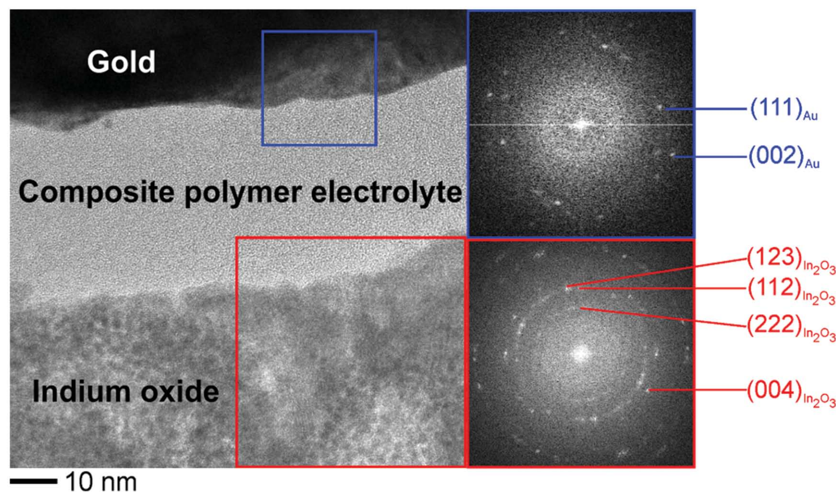

Figure 3. Cross-section TEM image of printed indium oxide/solid polymer electrolyte interface (the indium oxide precursor has been annealed at 400 °C for 2 h).

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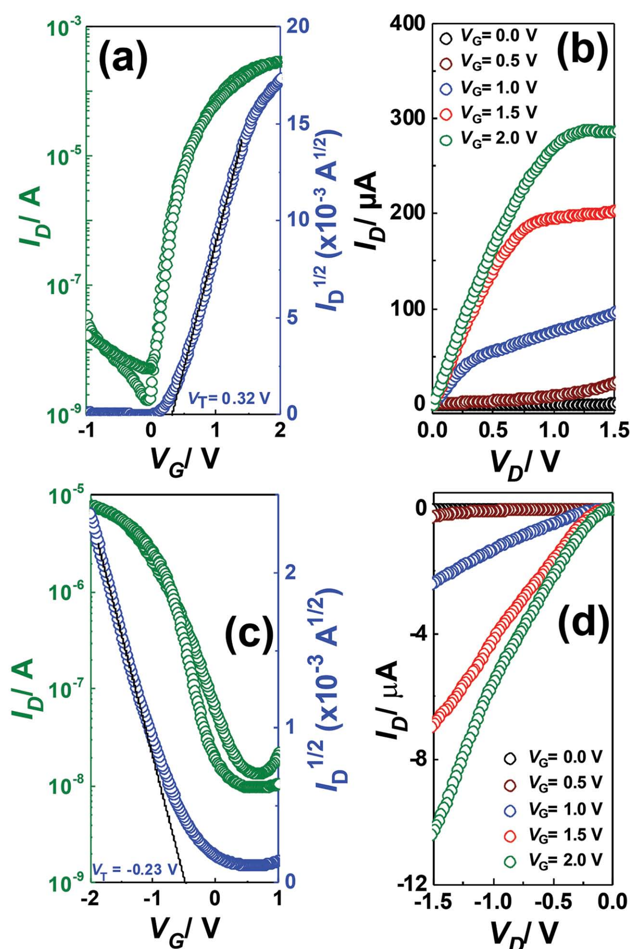

Figure 4. Transfer and current–voltage (*I–V*) characteristics of a,b) In_2O_3 channel NMOS and c,d) CuO channel PMOS FET, respectively.

$$I_{D,sat} = \frac{\mu_{FET} \times W \times C \times (V_G - V_T)^2}{2L} \quad (1)$$

where, $I_{D,sat}$ is the drain current in saturation regime, μ_{FET} is field effect mobility, V_G is gate voltage, V_T is threshold voltage, W is width, L is length of the channel, and the area specific capacitance (C), which is the double layer capacitance (C_{DL}) in our case. In order to calculate the C_{DL} value of the In_2O_3 thin films, separate FET devices (with identical W/L ratio and channel length of 100 μm) have been fabricated with sputtered ITO serving as the passive structure (drive electrodes). In this case, an accurate estimation of C_{DL} is possible by simply acquiring the displacement currents at different scan rates (Figure S8, Supporting Information). The calculated C_{DL} for In_2O_3 thin films is found to be 4.63 μF cm^{-2}. It is rather difficult to obtain the C_{DL} of CuO following this recipe; CuO must have pure metal electrodes, which in turn give large parasitic currents when in contact with the electrolyte (especially, due to the limited printing resolution, resulting in a large overlap area of printed electrolyte and metal contacts) which overwhelms the displacement currents from CuO. Therefore, in this case C_{DL} is estimated from parallel plate capacitors that have been built with large-area sputtered CuO thin films and Pt counter electrodes (Figure S9, Supporting Information). Here, the obtained capacitance value of CuO is around 3.2 μF cm^{-2}.

Although, PMOS FETs show limited performance, the CMOS logics have demonstrated fairly sound electrical characteristics, owing to the high performance of the NMOS devices and the well-matched threshold voltage (V_T) of the respective devices. The voltage transfer curve (VTC), the calculated signal gain (dV_{out}/dV_{in}) and the drive current through a typical CMOS inverter with 1.0 and 1.5 V supply voltage is shown in **Figure 5**. The CMOS inverter shows a maximum voltage gain of ≈21 at a drain supply voltage of 1.5 V. The drive current through the inverter is insignificant for the highest supply and input voltages, denoting very low static power dissipation. However, the dynamic power consumption of the device (P) being proportional to CV^2f (where, C = capacitance, V = supplied voltage, f = frequency)[2] is comparatively high in our case because of large specific capacitance (in the order of microfarads) of electrolytic insulator. Another important aspect of a CMOS inverter is the noise immunity for logic 1 (noise margin high, N_{MH}) and logic 0 (noise margin low, N_{ML}), in the ideal case both should

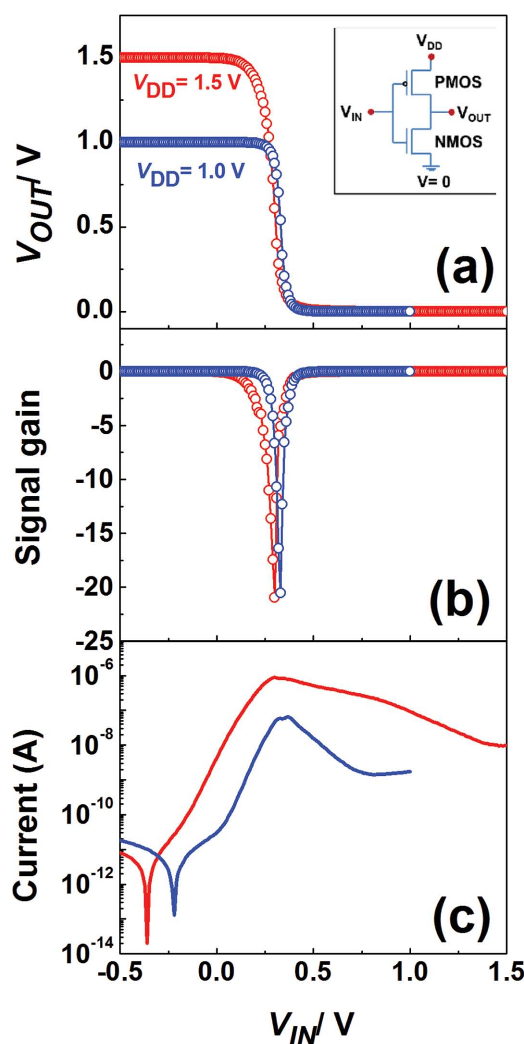

Figure 5. a) Voltage transfer characteristics, b) signal gain, and c) drive current through a typical CMOS inverter, respectively.

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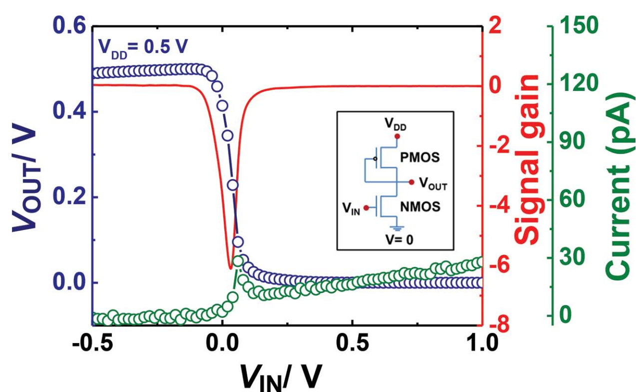

Figure 6. Transfer characteristic and signal gain of a typical CMOS common-source amplifier; markedly the supply voltage is only 0.5 V.

be equally high (Figure S10, Supporting Information). On the other hand, the undefined signal region (where the output signal is neither "1" nor "0") should be as small as possible; in present case these are found to be only 0.2 and 0.26 V for the supply voltage of 1 and 1.5 V, respectively. Next, once again combining one NMOS and one PMOS transistor, we demonstrate a common source amplifier, which can operate at a supply voltage of as low as 0.5 V, and shows a signal gain of 6 (**Figure 6**). Due to the low supply and input voltages, the C_{DL} is also not large in this case, resulting in a maximum drive current only in the picoampere range.

3. Conclusion

In summary, we have prepared ink-jet printed oxide CMOS electronics using precursor-derived indium oxide (NMOS) and copper oxide (PMOS) transistors, respectively. Composite solid polymer electrolyte has been used as the gate insulator, which prior to solidification, forms a highly conformal interface with the oxide semiconductor layer. The CMOS inverters that are built combining In_2O_3 NMOS and CuO PMOS FETs show complete rail-to-rail swing, sharp voltage transition and high signal gain at a very low supply voltage. The presented results indicate suitability of oxide transistors for printed circuits and possibility of battery compatible and portable electronic devices.

4. Experimental Section

Device Fabrication: Aqueous precursors for In_2O_3 and CuO were prepared separately by dissolving respective nitrate salts in de-ionized (DI) water. 0.05 M $In(NO_3)_3.xH_2O$ and 0.1 M $Cu(NO_3)_2.2.5H_2O$ were dissolved in DI water and glycerol (4:1 volume ratio) with continuous stirring until completely homogeneous solution was obtained. These as-prepared sols were then filtered through 0.2 µm polyvinylidene fluoride (PVDF) membrane syringe filter and used as the semiconductor inks for the FETs.

The devices were prepared on thermally oxidized silicon wafers (Si/SiO_2). The passive structures were fabricated from lithographically patterned, sputtered Cr(10 nm)/Pt(30 nm) electrodes. Both NMOS and PMOS transistors were prepared with an inplane FET geometry.[20] The channel lengths (L) of the NMOS and PMOS transistors were kept constant at 100 and 10 µm, respectively, while the channel widths ($W_{NMOS} \approx 100$ µm, $W_{PMOS} \approx 70$ µm) of the FETs were determined solely by the size of the printed channel layers. Therefore, for CMOS logics, the overall channel geometries of the PMOS and NMOS had been fixed to $(W/L)_p$:$(W/L)_n$ = 7:1. The overall CMOS inverter and amplifier geometries are shown in Figure S11, Supporting Information.

The oxide precursors and the composite solid polymer electrolyte were printed using Dimatix DMP 2831 desktop ink-jet printer. Ink-jet is a digital printing technique and extremely suitable for a large variety of functional inks, earlier reports have shown excellent quality of printed layers from different precursors or nanoparticulate inks.[28–30] The printed oxide precursors were dried at 150 °C for 2–3 min and subsequently annealed with a single annealing step in air at 400 °C for 2 h. The annealing temperature was far more than necessary for the In_2O_3 precursor (see Figure 1), however, for the sake of one step heating, such high annealing temperature was chosen as it was required for the CuO precursor. Nonetheless, the relatively high annealing temperature facilitated significant grain growth and excellent film quality of the NMOS, which at the end was translated into superior electrical performance.

Structural Characterization: The samples for GIXRD measurements were prepared by large area solution casting (10 × 10 mm^2) of indium and copper nitrate precursors. GIXRD measurements have been performed with a *Bruker D8 Discover* X-ray diffractometer with Mo-*Kα* target (50 kV, 50 mA) with a fixed incident angle of 0.4°. The morphology and surface roughness of the annealed films were analyzed using a *Leo 1530* scanning electron microscope and Bruker dimension icon atomic force microscope. To prepare the samples for the cross-section transmission electron microscopy analysis, first 50 nm of gold was sputtered then FEI Strata 400S dual beam FIB was used to prepare the cross-section sample. A selected area was coated with 10 nm of platinum with e-beam evaporation; next, 2 µm platinum was deposited using the gas injection ion beam system (GIS). Subsequently, a cross-section was prepared in the form of a thin lamella. For all the FIB procedures, different settings were used for milling and fine polishing depending on the size and thickness of the samples. Great care was taken to avoid beam-damage to the electrolyte system. Finally, a lamella of the stabilized cross-section was lifted out using an Omniprobe system and thinned for the TEM investigation. FEI Titan 80-300 microscope was used to image the cross-section morphology of the indium oxide and electrolyte interface.

Electrical Characterization: Electrical measurements were carried out using Agilent 4156C semiconductor parameter analyzer and Süss MicroTec, EP6 probe station. Electrochemical measurements were performed with *Metrohm* AUTOLAB 302 potentiostat equipped with low current measurement module.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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